

In the Claims

Claims 1-70 (cancelled).

Claim 71 (currently amended): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a ~~crystalline layer~~ structure comprising silicon and germanium;

a first transistor ~~device~~ supported by the ~~crystalline layer~~ structure, the first transistor ~~device~~ comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure ~~crystalline layer~~; ~~an entirety of the first active region within the crystalline layer being within a single crystal of the crystalline layer, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions;~~

a first layer of semiconductive material over the first transistor;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material formed physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor device supported by the first and second layers of semiconductive material, the second transistor device comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.

Claim 72 (original): The computer system of claim 71 wherein the second layer of semiconductive material is a crystalline layer ~~has~~ having a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the ~~crystalline layer~~ second layer of semiconductive material and the first second transistor device gate.

Claim 73 (original): The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon.

Claims 74 and 75 (canceled).

Claim 76 (original): The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon and germanium.

Claim 77 (canceled).

Claim 78 (original): The computer system of claim 72 wherein the entirety of the relaxed crystalline lattice is a single crystal.

Claim 79 (original): The computer system of claim 72 wherein the relaxed crystalline lattice is polycrystalline.

Claim 80 (original): The computer system of claim 72 wherein the relaxed crystalline lattice includes Si/Ge.

Claim 81 (original): The computer system of claim 80 wherein the relaxed crystalline lattice comprises from about 10 to about 60 atomic percent germanium.

Claims 82-88 (canceled).